SYSTEM FOR REDUCED POWER CONSUMPTION BY PHASE LOCKED LOOP AND METHOD THEREOF

ABSTRACT OF THE DISCLOSURE

A system and method are provided for reducing power consumption within a video processing portion of a system. Activity associated within a video-processing portion of a personal digital assistant is analyzed. As reduced activity is identified, power conservation modes are implemented. In a normal mode of operation, a clock signal generated through an external oscillator is provided to a phase locked loop (PLL). An output clock signal from the PLL is then provided to several dividers to generate system clock signals. In a reduced mode of operation, the output clock from the external oscillator is provided to a divider, bypassing the PLL. Video processing components then use clock signals based on the external oscillator. In a suspend mode, both the PLL and the external oscillator are disabled.